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CROSS-OVER VOLTAGE LOCK FOR DIFFERENTIAL OUTPUT DRIVERS

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BACKGROUND

Several types of wire based communication networks exist to provide communication among electronic devices. Many of these networks transmit a differential representation of the data over the network. A differential network uses a transmission cable that has a positive and a negative conductor, and positive and inverted representations of the data are sent on the conductors. A differential signal has the advantage of allowing faster data rates because the differential signals traverse lower voltage swings than single ended signals. Also, the data is less susceptible to noise in a differential signal bus because common mode signal noise picked up on the transmission cable is cancelled by sensing only the difference between the positive and negative conductors of the cable.

One critical parameter in differential signal wire based networks is the differential cross-over voltage of the signal transmitters. The differential cross-over voltage is the point where the voltage at the output of the positive signal transmitter crosses over with the voltage at the output of the negative signal transmitter. To minimize communication errors from power supply noise, electromagnetic interference (EMI), or signal ringing, the cross-over voltage should be at a point equidistant between the maximum and minimum voltages of the outputs. This point is often referred to as mid-rail.

If the network is a wire based serial network, transceivers are used to transmit and receive signals on the same transmission cable. Transmitters of wire based analog transceivers are generally designed with open-loop differential drivers. The drivers are open-loop in that they do not include a feedback mechanism in controlling their output. These transmitters are designed by tuning the cross-over voltage to an optimal mid-rail assuming a nominal process skew and nominal loading on the transmitter outputs. A problem with tuning is that when the transmitter is realized in silicon the cross-over voltage can deviate from the optimal

mid-rail value due to undesired process variations or due to asymmetric parasitic off-chip loading. A deviation in the cross-over voltage from the mid-rail voltage value can result in low yield in semiconductor fabrication of the transmitters. A mask iteration may be needed to take into account the non-nominal conditions and to re-tune the cross-over voltage to the mid-rail value.

What is needed is a differential transmitter with a self adjusting cross-over voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings like numerals refer to like components throughout the several views.

FIG. 1 is a drawing of a serial bus transceiver with an embodiment of a cross-over lock feedback circuit.

FIG. 2A is a graph showing an output transition of a transceiver with a weak pull-up circuit.

FIG. 2B is a graph showing asymmetry in the transitions of receiver outputs due to the weak pull-up circuit.

FIG. 3A is a graph showing an output transition of a transceiver with a weak pull-down circuit.

FIG. 3B is a graph showing asymmetry in the transitions of receiver outputs due to the weak pull-down circuit.

FIG. 4 is a drawing of a single ended driver for a differential transceiver.

FIG. 5 is a drawing of one embodiment of a switching network used in a cross-over lock feedback circuit.

FIG. 6 is a drawing of another embodiment of a switching network used in a cross-over lock feedback circuit.

FIG. 7A-C are graphs showing the cross-over lock feedback circuit correcting for weak pull-ups.

FIG. 8A-C are graphs showing the cross-over lock feedback circuit 110 correcting for weak pull-downs.

FIG. 9 is a drawing of a system using a differential transceiver to communicate over a transmission cable.

FIG. 10 is a flow chart of a method of providing a mid-rail cross-over voltage for a differential transceiver.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be used and structural changes may be made without departing from the scope of the present invention.

This document describes a feedback circuit for use with a differential transceiver that locks the cross-over voltage substantially to a point equidistant between the maximum and minimum voltage of the output of the transceiver transmitter. This equidistant point is often referred to as the mid-rail point.

FIG. 1 is a drawing of an embodiment of a serial bus transceiver 100 with a cross-over lock feedback circuit 110. The transceiver 100 allows a processor to communicate with other devices connected on the serial bus. The transceiver 100 includes a receiver 120 for receiving signals from a transmission cable 130 comprising a positive conductor 132 (D+) and a negative conductor 134 (D-). The receiver 120 comprises a differential receiver 122, a single ended receiver 124 for the positive conductor 132 (D+) and a single ended receiver 126 for the negative conductor 134 (D-). The single ended receivers 124, 126 detect rail-to-rail transitions on the D+, D- conductors 132, 134 and trip when a voltage threshold on the differential inputs is exceeded. The single-ended receivers 122, 124 are used to detect events such as idle mode or wake-up on the serial bus, and to determine a data transfer rate. The differential receiver 122 detects the incoming data stream and the output trips at the cross-over voltage of the D+, D- conductors 132, 134.

The transceiver 100 also includes a transmitter 140 for transmitting signals on the transmission cable 130. The transmitter 140 comprises a single ended output

driver 142 for the positive conductor 132 and a single ended driver 144 for the negative conductor 134. If the transceiver 100 is implemented in CMOS, output drivers 142, 144 are typically designed with PMOS pull-ups and NMOS pull-downs that have equal strength at nominal conditions.

FIG. 2A is a graph 210 showing an output transition of a transceiver 100 with a weak pull-up circuit. In the embodiment shown, the signals transition between a low rail of zero volts and a high rail of three volts. Other values for low and high rails are within contemplation of this application. The D+ conductor 132 is shown transitioning from the high rail to the low rail, and the D- 134 conductor is transitioning from the low rail to the high rail. Because of the mismatch in pull-up rise time and pull-down fall time, a high-to-low signal transition 212 occurs more quickly than a low-to-high signal transition 214. The result is a cross-over voltage point 216 at about one volt instead of the mid-rail 1.5 volts. The differential receiver 122 has high gain and trips at the cross-over point. Because the cross-over point is low, the transceiver is more susceptible to noise on the low rail conductor than if the cross-over point was mid-rail.

FIG. 2B is a graph 220 showing asymmetry in the transitions of receiver outputs 222, 224, 226 due to the weak pull-up circuit. In the embodiment, the output of the differential receiver 222 (RXD) follows the positive logic of the output of the positive single ended receiver 224 (RXDP) which follows the transition of the D+ conductor 132. The output of the negative single ended receiver 226 (RXDM) follows the D- conductor 132. The graph 220 shows the output of the differential receiver 222 (RXD) trips before the output of the negative receiver 226 (RXDM). In the ideal case of a mid-rail cross-over point, the single ended receiver 224, 226 transition points would be coincident or symmetric about the differential receiver 222 output transition point. For the opposite case when the D+ conductor is transitioning from low to high, the output of the positive receiver 224 (RXDP) lags the output of the differential receiver 222 (RXD).

FIG. 3A is a graph 310 showing an output transition of a transceiver 100 with a weak pull-down circuit. As in FIG. 2A, the D+ conductor 132 is shown

transitioning from the high rail to the low rail, and the D- conductor 134 is transitioning from the low rail to the high rail. This time, the mismatch in rise and fall times causes a cross-over voltage point 316 at about two volts instead of the mid-rail 1.5 volts. Because the cross-over point is high, the transceiver is more susceptible to noise on the high rail conductor. FIG. 3B is a graph 320 showing asymmetry in the transitions of receiver outputs 322, 324, 326 due to the weak pull-down circuit. The graph 320 shows the output of the differential receiver 322 (RXD) trips before the output of the positive receiver 324 (RXDP). For the opposite case when the D+ conductor is transitioning from low to high, the output of the negative receiver 326 (RXDM) lags the output of the differential receiver 322 (RXD).

To correct the mismatches in rise and fall times, the cross-over feedback lock circuit 110 creates a bias voltage to correct the strength of the pull-down and/or pull-up circuits in the transmitter single ended output drivers 142, 144. An embodiment of a single ended output driver 400 is shown in FIG. 4. Changing the voltage on the gate of PMOS transistor 410 changes the current drive strength of the pull-up bias circuit of the output driver 400. For example, if the voltage of the gate is decreased, the drive strength of the PMOS transistor 410 is increased, and the pull-up is biased toward the high rail (VCC). Conversely, if the gate voltage is increased, the drive strength of the PMOS transistor 410 is decreased, and the pull-up is biased away from the high rail.

Changing the voltage on the gate of NMOS transistor 420 changes the bias of the pull-down of the output driver 400. For example, if the voltage of the gate is increased, the drive strength of the NMOS transistor 420 is increased, and the pull-down is biased toward the low rail (VSS). Conversely, if the gate voltage is decreased, the drive strength of the NMOS transistor 420 is decreased, and the pull-down is biased away from the low rail. Thus, a closed loop system is created by feeding back a voltage to the gates that adjusts the pull-up and/or pull-down biasing by an amount that corrects the mismatch in drive strength.

To create the correcting voltage, a charge is produced based on the output switching time of the differential receiver 122 in relation to the output switching time of the single ended receivers 124, 126. If the cross-over voltage is at mid-rail, the switching is symmetric and no net charge is produced. If the cross-over voltage is not at mid-rail the deviation of the cross-over voltage from a predetermined level results in switching that is asymmetric, and the asymmetry produces a net charge that is converted into a correcting bias voltage for the output drivers 142, 144.

One embodiment of a switching network 500 to create this charge is shown in FIG. 5. The embodiment comprises a P-bias compensation circuit 505 to compensate the PMOS pull-up circuits of the single ended output drivers 142, 144 and an N-bias compensation circuit 545 to compensate the NMOS pull-down circuits of the single ended output drivers 142, 144. The compensation circuits 505, 545 create a correcting bias voltage by adjusting a charge on a capacitor 510, 550.

For the P-bias circuit 505, combinational logic 515, 516 enables switches 520, 525 to either add charge or remove charge from the capacitor 510 by enabling current to flow to or from the capacitor 510. The switching to enable the current is a function of the states of the outputs of the differential receiver (RXD) 530 and the D+ single ended receiver (RXDP) 535. This function can be expressed as an equation in terms of RXD and RXDP as:

$$I \propto F(\overline{RXD} \bullet RXDP) - G(RXD \bullet \overline{RXDP})$$

If the output of the differential driver 122 lags the output of the D+ single ended receiver 124, the pull-up bias is too strong. The gate voltage of the PMOS transistor 410 of the single ended output drivers 142, 144 is adjusted higher to weaken the pull-up by adding more charge to the capacitor 510 by enabling current to flow through switch 520. Thus, switch 520 is enabled and current is pushed onto capacitor 510 during the time when RXD is low while RXDP is high. The time duration 330 that this logic state of the receivers 122, 124, 126 is valid is shown in FIG. 3B.

If the output of the differential driver 122 leads the output of D+ single ended driver 124, the pull-up bias is too weak. The gate voltage of the PMOS

transistor 410 of the single ended output drivers 142, 144 is adjusted lower to strengthen the pull-up by reducing the charge on the capacitor 510 by enabling switch 525. Thus, switch 525 is enabled and drains current from capacitor 520 during the time when RXD is high while RXDP is low. The time duration 230 that this logic state of the receivers 122, 124, 126 is valid is shown in FIG. 2B. Neither switch 520, 525 is enabled while RXD and RXDP are in the same state.

For the N-bias circuit 545, combinational logic 555, 516 enables switches 560, 565 to either add charge or remove charge from the capacitor 550 by allowing current to flow to or from the capacitor 550. The switching to enable the current is a function based on the states of the outputs of the differential receiver (RXD) 570 and the D- single ended receiver (RXDM) 575. This function can be expressed as an equation in terms of RXD and RXDM as:

$$I \propto F(RXD \bullet RXDM) - G(\overline{RXD} \bullet \overline{RXDM})$$

If the output transition of the differential driver 122 lags the output transition of the D- single ended receiver 126, the pull-down bias is too strong. The gate voltage of the NMOS transistor 420 of the single ended output drivers 142, 144 is adjusted lower to weaken the pull-down by reducing charge to the capacitor 550 by enabling switch 565. Thus, in one embodiment switch 565 is enabled and drains current during the time when RXD is low while RXDM is low. This time duration 240 is shown in FIG. 2B.

If the output of the differential driver 122 leads the output of D- single ended driver 126, the pull-down bias is too weak. The gate voltage of the NMOS transistor 420 of the single ended output drivers 142, 144 is adjusted higher to strengthen the pull-up by increasing the charge on the capacitor 550 by enabling switch 560. Thus, in one embodiment switch 560 is enabled during the time when RXD is high while RXDM is high. This time duration 340 is shown in FIG. 3B. Neither switch 560, 565 is enabled while RXD and RXDM are in opposite states.

FIG. 6 shows an embodiment of a switching network using transmission gate, or pass gate, switches 610. The combinational logic is implemented by enabling the pass gate switches 610 in series. For example switch 560 of FIG. 5 is

implemented by enabling two pass gate switches with outputs RXD and RXDM. In other embodiments, the combinational logic is implemented with straightforward logic circuits such as and-gates and inverters. One of ordinary skill in the art would understand, upon reading and comprehending this disclosure, that various embodiments of the combinational logic include various combinations of the illustrated circuits and variations of the high and low logic states.

FIG. 7A-C are graphs showing the cross-over lock feedback circuit 110 correcting for weak pull-ups. FIG. 7A shows the initial low crossover voltage (about one volt) on the D+ and D- outputs of the single ended transceiver drivers. FIG. 7B shows the feedback circuit 110 applying a correcting voltage to the transmitter 140 pull-up and pull-down circuits. FIG. 7B also shows that the correcting voltage is adjusted on a clock period basis because the charge is produced from transitions on the transmission cable 130 detected by the receivers 122, 124, 126. After about twenty clock periods, the cross-over voltage is brought back to mid-rail (1.5 Volts) as shown in FIG. 7C.

FIG. 8A-C are graphs showing the cross-over lock feedback circuit 110 correcting for weak pull-downs. FIG. 8A shows the initial low crossover voltage is higher than mid-rail (about two volts). FIG. 8B shows the feedback circuit 110 applying a correcting voltage to the transmitter 140 pull-up and pull-down circuits. After about twenty clock periods, the cross-over voltage is brought back to mid-rail (1.5 Volts) as shown in FIG. 8C.

FIG. 9 is a drawing of a system 900 that uses a differential transceiver interface 905 to communicate over a transmission cable 930. System 900 includes receiver 920, driver 940, processor 960, memory 970, transceiver controller 950 and crossover feedback lock circuit 910. Receiver 920 includes single ended receivers 924, 926 and differential receiver 922 to detect signals on nodes 932, 934. Differential driver 940 includes a single ended driver for node 932 and single ended driver for node 934. Crossover lock feedback circuit 910 corrects deviations of the cross-over voltage on transmission cable 930 from a point equidistant between the maximum and minimum output voltages of driver 940.

Transceiver controller 950 communicates with other devices connected to node 932, 934 by transmitting data on driver 940 and receiving data on receiver 920. The transceiver controller 950 also communicates with microprocessor 960 and memory 970. The transceiver controller 950 can be any type of transceiver controller suitable for communication with the transceiver interface 905. For example, transceiver controller 950 may be a universal serial bus, a synchronous optical network (SONET), a Firewire controller, or the like.

Processor 960 can be any type of processor suitable for operation with the system 900. For example, in various embodiments of the system 900, processor 960 is a microprocessor, a microcontroller or the like. Memory 970 represents an article that includes a machine accessible medium. For example, memory 970 may represent any one or a combination of the following: a hard disk, a floppy disk, random access memory (RAM), read only memory (ROM), flash memory, CDROM, or any other type of article that includes a medium readable by a machine.

Systems represented by the foregoing figures can be of any type. Examples of represented systems include computers (e.g., desktops, laptops, notebooks, handhelds, servers, Web appliances, routers, etc.), wireless communication devices (e.g., cellular phones, cordless phones, pagers, personal data assistants, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, digital video disc players, camcorders, digital cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games, watches, etc.), and the like.

Transmission cable 930 can be any type of two conductor cable suitable for operation with the system 900. For example, in various embodiments of the system, transmission cable 930 is a coaxial cable, a twisted pair cable, and the like.

FIG. 10 is a flow chart of a method 1000 of providing a mid-rail cross-over voltage for a differential transceiver. At 1010, a difference is measured between a voltage at which output voltages of first and second differential drivers of a differential signal transceiver cross-over and a point substantially equidistant

between maximum and minimum output voltages. At 1020, a correcting bias voltage is provided that is proportional to a difference between the cross-over voltage and the equidistant voltage. At 1030, the correcting bias voltage is applied to the differential drivers to vary the point where the first and second output voltages cross-over.

Although specific examples have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement calculated to achieve the same purpose could be substituted for the specific example shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents shown.